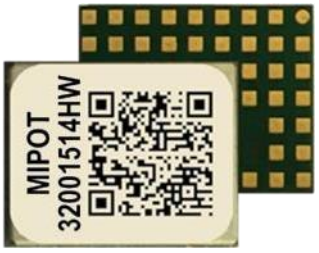
Wireless Protocol Modules MiP Series 32001514HW

Hardware Only Radio Module with MCU

Datasheet



Overview

The 32001514 is a transceiver operating in the 868 and 915 MHz SRD Band; thanks to its very stable TCXO and to its high output power up to 20 dBm it is optimized for very long range, high interference immunity and low power applications, suitable for LPWA networks.

The module supports LoRa®, (G)FSK, (G)MSK and BPSK modulations, compatible with standardized or proprietary protocols such as LoRaWAN®, Sigfox™, W-MBus and more

(fully open wireless system-on-chip).

The 32001514 features a dual core microcontroller, based on the STM32WL55J, in which one is dedicated to the radio stack and the ARM Cortex M4 is free for the customer application firmware.

Thanks to its small LGA form factor (11.3 x 8.9 mm only) and its low current consumption, this module allows the implementation of highly integrated low power (battery operated) solutions for Internet of Things (IoT) applications, security systems, sensor networks, metering, smart buildings, agriculture, supply chain.

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1. Product Features

Mechanical highlights:

- ✓ Extremely compact dimensions
- ✓ LGA pattern

Low power characteristics:

- ✓ Sleep current consumption 2.2 µA
- ✓ 11 mA in RX mode

Memories:

- ✓ 196 Kbyte Flash memory
- ✓ 32 Kbyte RAM
- ✓ 512 byte OTP (One Time Programmable) memory

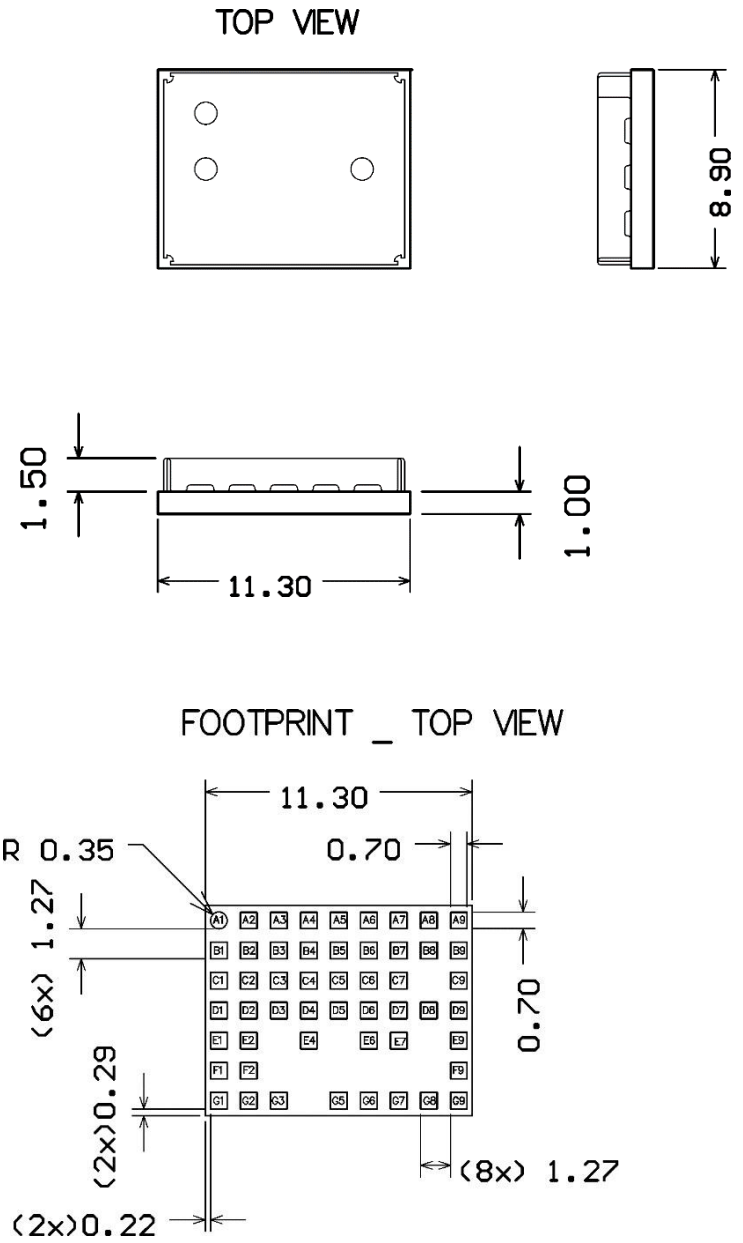
RF performances:

- ✓ -135 dBm Sensitivity (@LoRa)
- ✓ 20 dBm Output power

Additional features:

- ✓ ARM Cortex-M4 CPU
- ✓ Internal communication channel with the radio peripheral
- ✓ Based on STM32WL55J
- ✓ 32 MHz TCXO
- ✓ Modulation: LoRa®, (G)FSK, (G)MSK, BPSK
- ✓ -40 °C ÷ 85 °C temperature range

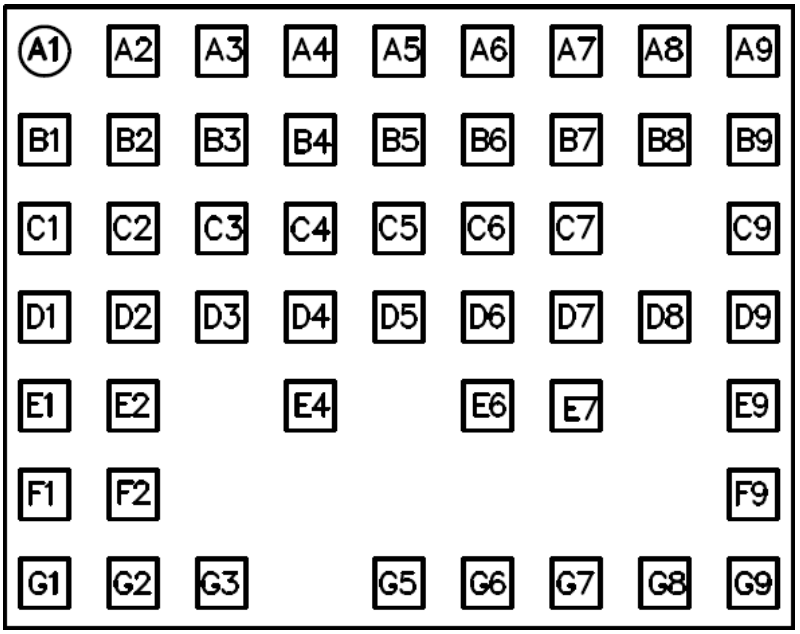
2. Mechanical Dimensions



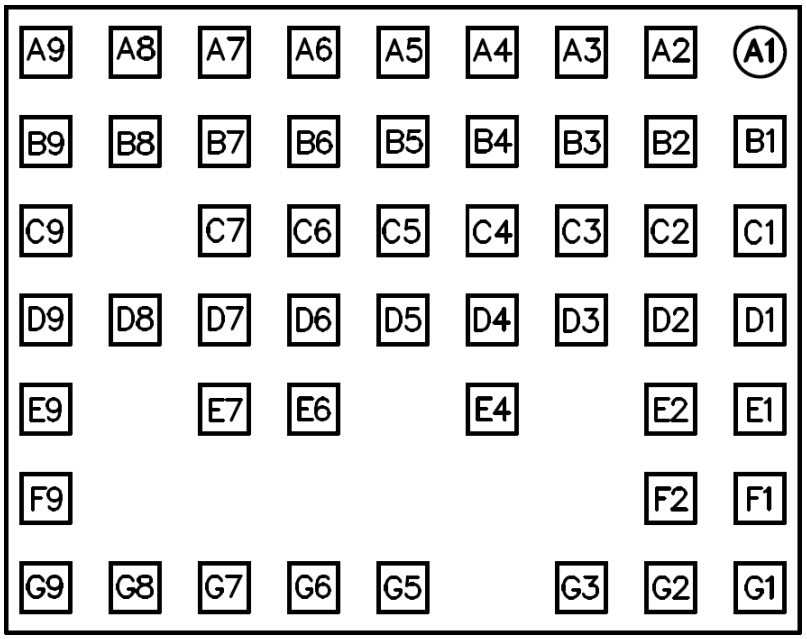
Note: Dimension in mm. General tolerance ±0.1 mm. The tolerance is not cumulative

3. Pad Definition

Top View



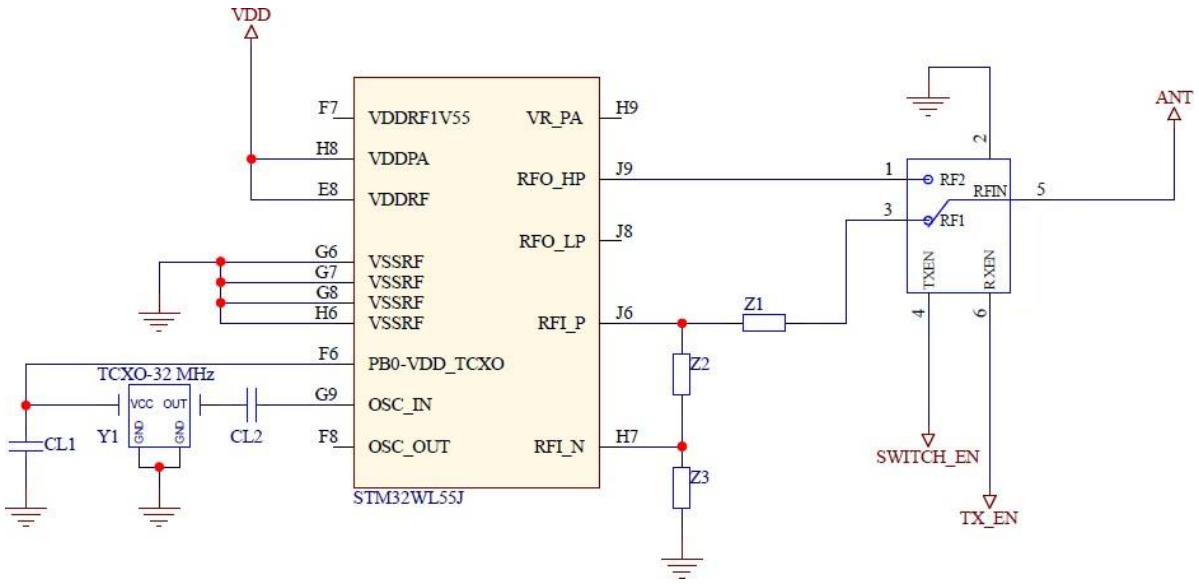
Bottom View

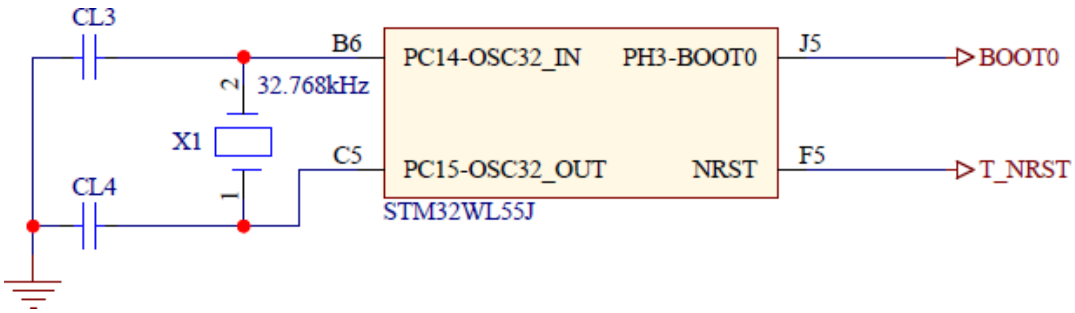


32001514HW LGA PAD	STM32WL BGA BALL
A1	PA6
A2	PA5
A3	PA4
A4	PC0
A5	PC1
A6	PB5
A7	PB8
A8	PB9
A9	VDD
B1	PA7
B2	PC6
B3	PA2
B4	PA3
B5	PB6
B6	PB7
B7	PA15
B8	VDDA
B9	VDD
C1	PH3-BOOT0
C2	PA8
C3	PA1
C4	GND
C5	PA0
C6	PB4
C7	VREF+
C9	GND

32001514HW LGA PAD	STM32WL BGA BALL
D1	GND
D2	PB10
D3	PB11
D4	GND
D5	PB14
D6	PA10
D7	VBAT
D8	PB13
D9	PC2
E1	GND
E2	GND
E4	PB1
E6	PB2
E7	PA12
E9	PC3
F1	ANT
F2	GND
F9	PB12
G1	GND
G2	GND
G3	GND
G5	NRST
G6	SWDIO
G7	SWCLK
G8	SWO
G9	PA9

4. Internal Hardware Overview





4.1. High Frequency Clock

System clock is provided by an ultra-stable 32 MHz TCXO, connected to the module pad G9 (STM32WL55J signal OSC-IN) and fed by the pin F6 (STM32WL55J signal PB0-VDD_TCXO) set to high.

The 32 MHz TCXO has ±1 PPM frequency tolerance at room temperature and ±2.5 PPM frequency stability over the operative temperature range (-40 °C ÷ 85 °C).

4.2. Low Frequency Clock and RTC feature

Low Frequency Clock and Real-Time Clock feature is provided by an external 32.768 kHz crystal, connected to module pads B6 and C5 (STM32WL55J signal PC14-OSC32_IN and PC15_OSC32_OUT).

The 32.768 kHz TCXO has ±20 PPM frequency tolerance at room temperature.

4.3. MCU peripherals and reserved pads

All STM32WL55J MCU peripherals can be used and freely configured.

Some balls of the STM32WL55J are reserved for internal use, so those are not available for the user application and must be not modified in any way:

- PA11
- PC4
- PC13
- PB0
- PC5
- PC15

4.4. Radio port switching

The radio embedded on the STM32WL55J uses the high power output with an internal PA.

Switching between transmission and reception is achieved via a RF switch controlled by the following STM32WL55J ports:

PC4	PC5	State
0	X	RF switch disabled
1	0	RX enabled
1	1	TX enabled

4.5. Internal power supply regulator

In order to proper supply the microcontroller, use the *LDO Supply* configuration.

5. Hardware integration

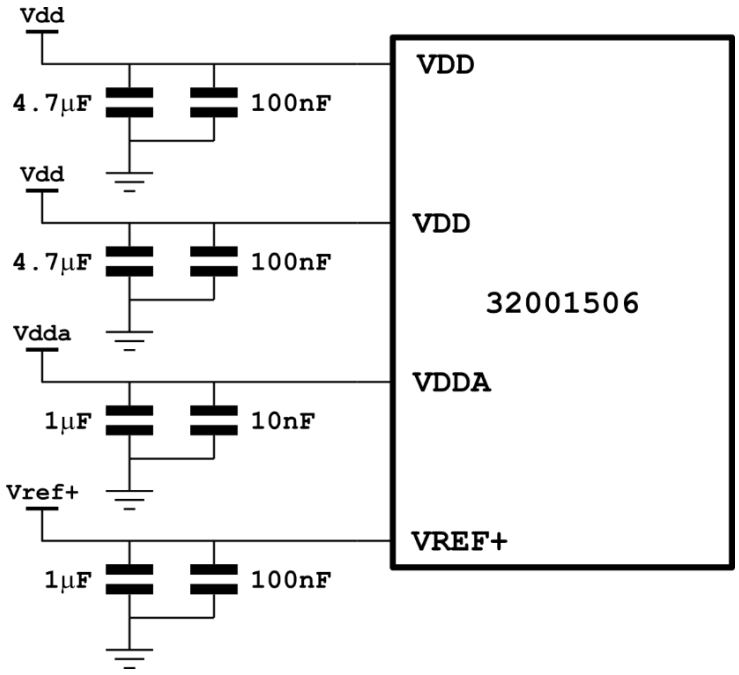
5.1. Layout guidelines

For better noise rejection, put the decoupling capacitors as close as possible to the power pads of the module, giving precedence to the low value ones.

The trace connecting to the RF pin must have an impedance of 50 Ω. For better performance, connect the GND pads around the RF pad without thermals.

5.2. Decoupling capacitors

Each power supply pad must be decoupled with capacitors with the values suggested in the figure.



6. Firmware development

The 32001514 module is based on the STM32WL55J and embeds the necessary circuitry for the RF subsystem in the 868 and 915 MHz band.

The MCU employs an asymmetrical dual core CPU comprised of an ARM Cortex-M4 and an ARM Cortex-M0+.

The Cortex-M0+ core can be reserved for the RF stack while the application firmware runs on the Cortex-M4. The communication between the cores is done using the Inter-Processor Communication Controller (IPCC).

For details about the MCU, please refer to STM32WL55J data sheet (DS13293) and reference manual (RM0453).

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Parameter	Max.	Unit
Supply Voltage (VDD)	3.9	V
Radio Frequency Input Level, pin F1	0	dBm
Voltage Standing Wave Radio (VSWR) at RF Input, ANT, pad F1	10:1	
I/O Pin voltage	VDD + 0.3	V
Storage Temperature	-40 ÷ 100	°C
Operating Temperature	-40 ÷ 85	°C

7.2. Operating Condition

Note: All RF parameters measured with input (pad F1, ANT) connected to a 50 Ω impedance signal source or load.

7.2.1. GENERAL ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
Supply Voltage (VDD)	1.9	3.0	3.6	V	
VDDA	0	-	3.6	V	
VBAT	1.55	-	3.6	V	
VIN	-0.3	-	VDD+0.3	V	
Sleep DC Current	-	2.2	3.0	µA	
Data Rate 2-FSK	-	-	50	kbit/s	
Data Rate LoRa®	0.25	-	11	kbit/s	

7.2.2. RECEIVER ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
DC Current Drain	-	-	11	mA	6
Operating Frequency	850.0	-	928.0	MHz	
Channel Frequency Precision	-	±15	-	kHz	
Sensitivity, 2-FSK	-	-115	-	dBm	2,3,5
Sensitivity, LoRa®	-	-135	-	dBm	2,4,5
Image Frequency Rejection	-	54	-	dB	7
Spurious radiated level	-	-	-57	dBm	
Output Logic Low	GND	-	0.05	V	
Output Logic High	VDD-0.2	-	VDD	V	

7.2.3. TRANSMITTER ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
Current Drain (CW @14dBm)	-	103	-	mA	1,2
Operating frequency	850.0	-	928.0	MHz	
Occupied Bandwidth	-	125	-	kHz	
Operating Channel Width	-	200	-	kHz	
Maximum Output power (50 Ω load)	-	14	20	dBm	1,2,10
RF Output Impedance	-	50	-	Ω	
Input Logic Low	GND	-	0.05	V	
Input Logic High	VDD-0.2	-	VDD	V	

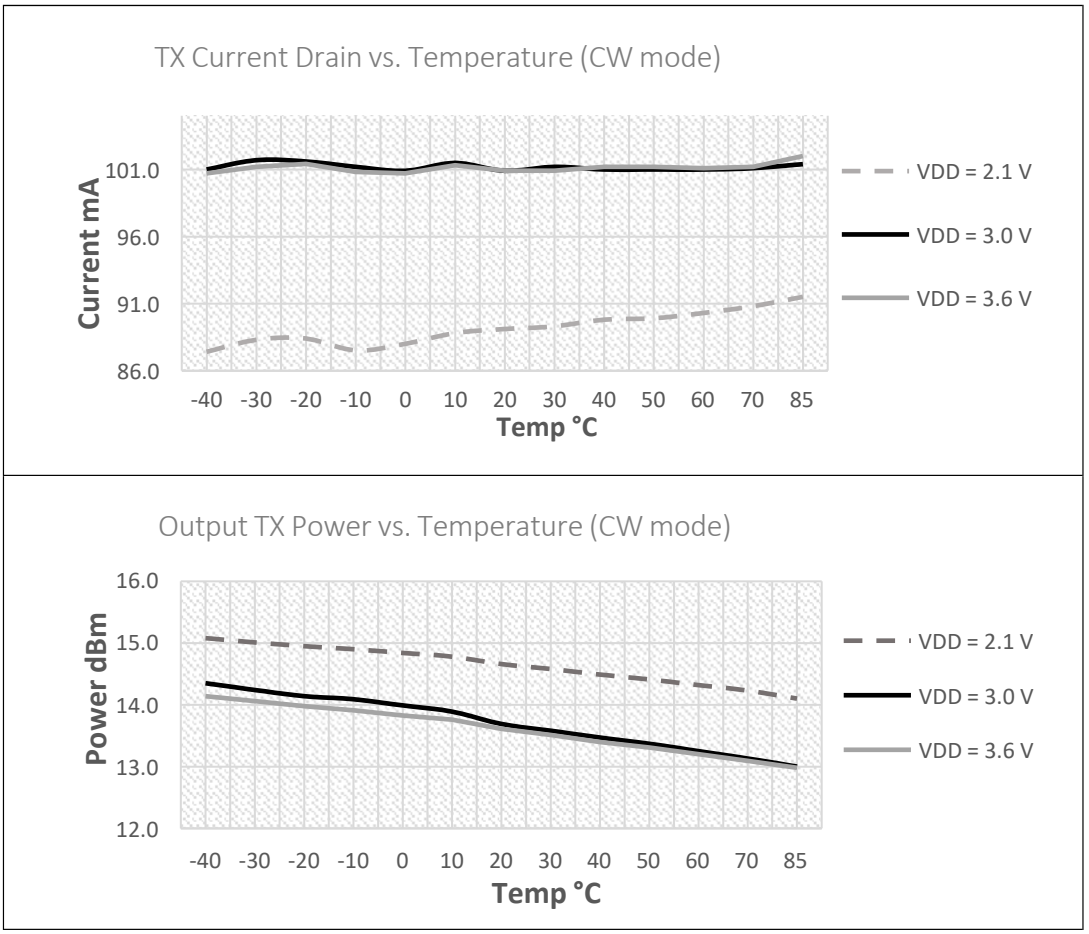
Notes:

1) VDD = 3.6 V.
2) All RF parameters measured with input (pin F1, ANT) connected to 50 Ω impedance signal source or load.
3) Pseudo random code NRZ, 2-FSK BER (bit error rate) = 0.1 % or better, 2-level FSK modulation without pre-filtering, Bit Rate = 4.8 kbit/s, frequency deviation = 5 kHz, filter bandwidth = 20 kHz
4) LoRa® PER (packet error rate) = 1 %, packet of 64 bytes, preamble of 8 bytes, error correction code CR = 4/5, CRC on payload enabled, no reduced encoding, no implicit header.
5) Sensitivities given using highest LNA gain step.
6) Power consumption measured with -140 dBm signal and AGC ON.

7) Blocking immunity, ACR and co-channel rejection, given for a single tone interferer and referenced to sensitivity +6 dB, blocking tests performed with unmodulated signal measured as per ETSI 300 220-1.
8) Time by power-on to valid data reception.
9) Time by test signal at RF input to valid data reception.
10) In order to not exceed the maximum power permitted by the ETSI EN 300 220 regulation, choose an appropriate antenna system and power supply.

8. Temperature Range Curves

Note: All RF parameters measured with input (pad F1) connected to a 50 Ω impedance signal source or load.



9. Supporting documentation

Title	Description	Doc
Manufacturing Process Information for LGA MiP Series Modules	Packaging information, Tape& Reel Specification, Reflow soldering information	AN_MNF002
STM32WL55J data sheet	Overview of the MCU and its peripherals	DS13293 (from ST)
STM32WL55J reference manual	Detailed description of the MCU and its peripherals	RM0453 (from ST)

10. Ordering Information

Title	Description	DoC
32001514HW	MiP Series Hardware Only	N/A

11. Revision History

Revision	Date	Description
0.0	08.02.2024	First emission