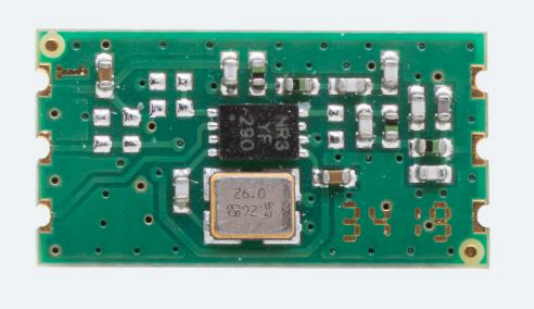
# **32001371 -** SMD 433.92MHz OOK/FSK TRANSMITTER



32001371 TX module is an SMD 433.92MHz OOK-FSK transmitter. It can operate in:

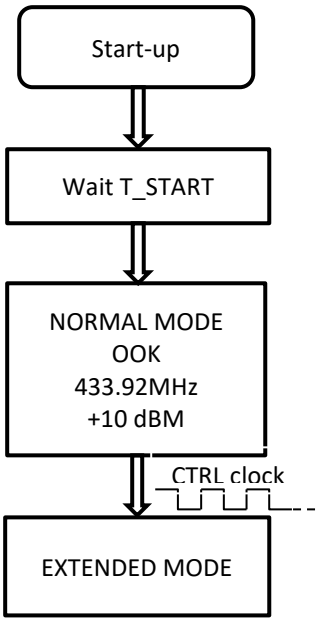
- **NORMAL Transmission Mode** whose operation is already described in the datasheet
- **EXTENDED Mode**, user programmable, covered in this document

## 1. EXTENDED MODE

Extended mode can be entered using a **2 wire interface** provided by means of the same I/O lines that are used for normal operation. Such lines are available on pins 2 and 3 and must be connected to an external microcontroller. Pin 2 is used as CTRL pin for configuration and is normally connected to Vcc for standard transmission mode while pin 3 is TX DATA pin.

## 1.1. Start-up

Following flow chart shows start-up sequence.




At power up the 32001371 TX module waits T_START time to elapse and then automatically starts in NORMAL MODE with OOK modulation at 433.92MHz. It can work indefinitely in NORMAL MODE or it can switch to EXTENDED MODE.

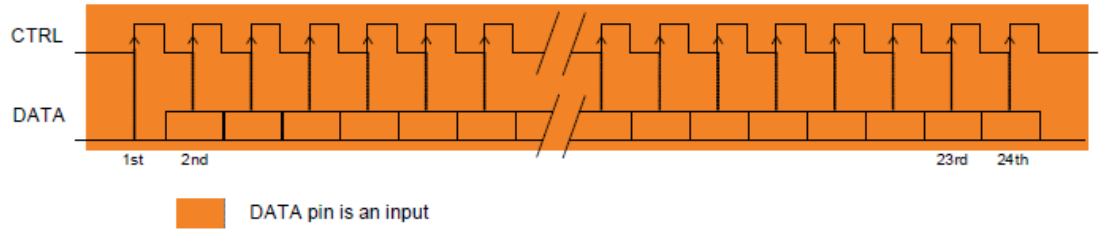
## 1.2. EXTENDED Programming mode

EXTENDED Programming mode can be entered after start-up from NORMAL MODE.

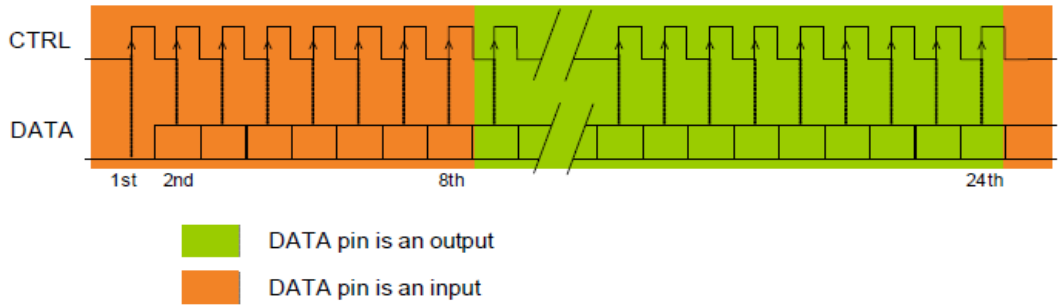
As long as CTRL (pin 2) is kept stable, the TX DATA (pin 3) pin is considered by the circuit as the input for the data to be transmitted over the air. Programming mode is entered providing a square wave (up to 10MHz) on CTRL pin and holding TX DATA pin low during a CTRL's rising edge.

Once programming mode is entered TX module's internal registers are available both for writing and reading operations. All commands are 24 bits long as shown in following images.

*Write operation:*




*Read operation:*




As stated in previous discussion, programming of the configuration register is triggered by a rising edge on the CTRL line while TX DATA line is held low. Upon detection of such condition, the data applied to the TX DATA pin is accepted as register configuration information, the data bits are clocked on subsequent rising edges of the clocking signal applied to the CTRL pin. Note that, **once triggered, all 24 clock cycle must be issued to the 32001371 TX module**.

The first rising edge on CTRL which initiates the programming mode must occur **at least 1 ms after** the circuit has been powered up or reset.

Following table lists available configuration commands:

| Byte 0 | | | | | | | | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Instruction |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | (0000) | | | | DA(15:0) | | | | | | | | | | | | | | | | Write Application bits |
| 0 | 0 | 0 | 1 | 1 | | | | DF(18:0) | | | | | | | | | | | | | | | | Write Frequency bits |
| 0 | 0 | 1 | 1 | (0011) | | | | DA(15:0) | | | | | | | | | | | | | | | | Read Application bits |
| 0 | 1 | 0 | 0 | (0100) | | | | DF(15:0) | | | | | | | | | | | | | | | | Read 16 least significant Frequency bits |
| 0 | 1 | 0 | 1 | (0101) | | | | DS(12:5) | | | | | | | | DS(4:0) | | | | | | | | DF(18:16) Read Radio chip version, Status and 3 most significant Frequency bits |
| 0 | 1 | 1 | 0 | (0110) | | | | DS(28:13) | | | | | | | | | | | | | | | | Read Bits signature |
| 1 | x | | | | | | | | | | | | | | | | | | | | | | | Discard, not a valid instruction |
| All 1 | | | | | | | | | | | | | | | | | | | | | | | | Recovery instruction |

The first “0” transmitted to the 32001371 TX module is required to initialize communication. The following 3 bits (highlighted in blue) determine the type of instruction. The forthcoming bits (highlighted in green) define a protection pattern; any error in these bits voids the instruction.

### 1.2.1. APPLICATION Configuration Parameters

| Name | Number | Description | NORMAL MODE |
|---|---|---|---|
| Mode | DA[15] | Mode:<br>0 -> Automatic mode<br>1 -> Forced transmit mode | 0 |
| Modul | DA[14] | Modulation scheme:<br>0 -> FSK<br>1 -> OOK | 1 |
| Band | DA[13] | Must be 0 | 0 |
| Fdev | DA[12:5] | RF Frequency deviation in FSK mode only. Expressed in multiples of $F_{step}$ = 1.58691kHz | Unused |
| Pout | DA[4] | Output power range:<br>0 -> 0 dBm<br>1 -> 10 dBm | 1 |
| TOFFT | DA[3] | Period of inactivity on TX DATA before 32001371 TX module enters Sleep mode in Extended mode:<br>0 -> 2 ms<br>1 -> 20 ms | 1 |
| RES | DA[2:0] | Reserved | 100 |

Note: All changes to the APPLICATION parameters must be performed when the device is in Sleep mode, with the exception of DA[15]. Mode can be sequentially written to “1”, and then “0” while the device is in Transmit mode, to speed up the turn off process and circumvent the TOFFT delay.

### 1.2.2. FREQUENCY Configuration Parameters

| Name | Number | Description | NORMAL MODE |
|---|---|---|---|
| $F_{rf}$ | DF[18:0] | RF operating frequency | 0x42C1C<br>Frf=433.92MHz |

If done in Sleep mode, the Frequency change instruction will be applied next time the 32001371 TX module is turned on. If Frequency change occurs during transmission, the automated Frequency Hopping sequence will take place.

### 1.2.3. Status Parameters

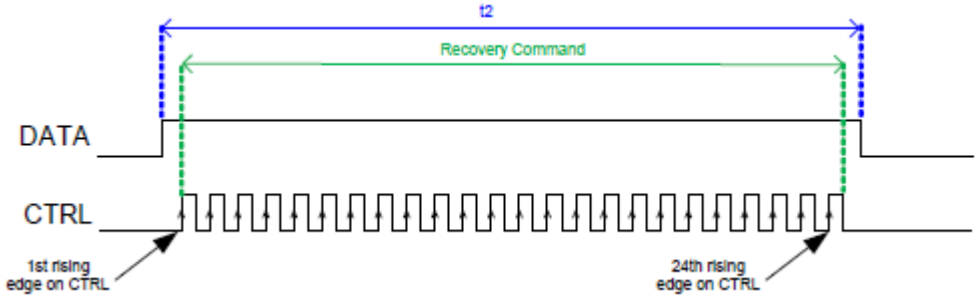
| Name | Number | Description | Normal and Extended modes |
|---|---|---|---|
| RES | DS[28:13] | Reserved | - |
| Radio chip Version | DS[12:5] | Radio chip identification number | "0001 0001" --> V1A |
| RES | DS[4:2] | Reserved | - |
| TX_READY | DS[1] | TX_READY:<br>0 -> Transmitter not Ready<br>1 -> Transmitter is Ready | - |
| RES | DS[0] | Reserved | - |

Chip Version DS[12:5] are read-only bits.

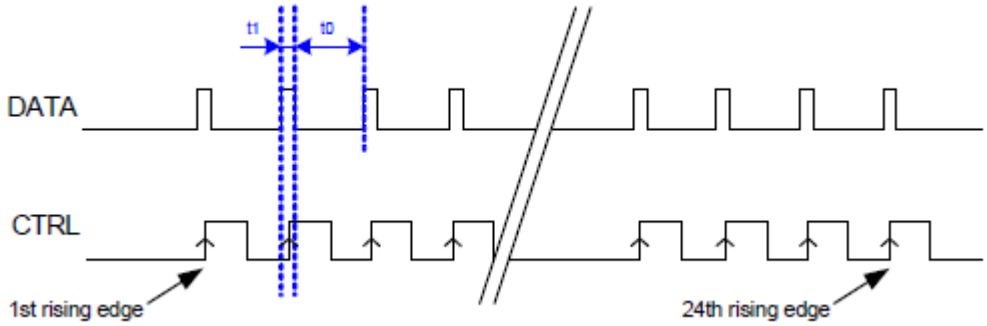
### 1.2.4. Recovery Command

In the event of spurious activity (less than 24 clock cycles received) on the CTRL pin, control over the 2 wire interface can be recovered in two possible ways:

*Quick Recovery command:*



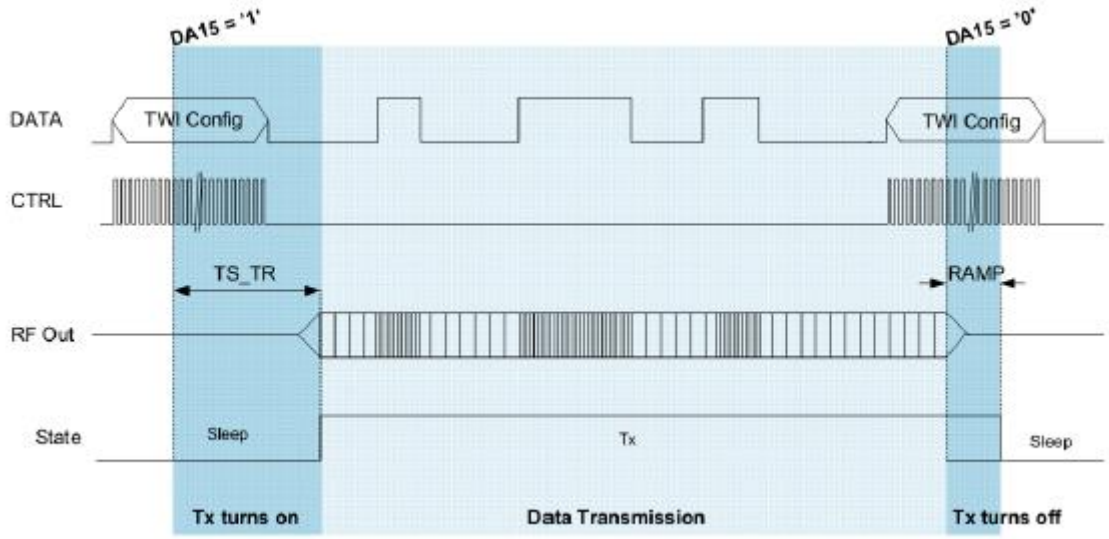

*Pulsed Recovery command:*




- If $t_2$ < 5 us, the 32001371 TX module will not turn into TX mode during the recovery command (if not previously in TX mode)
- If $t_1$ < 5 us, with $t_0$ > 5 us, the 32001371 TX module will not turn into TX mode in the second scenario of recovery command
- During the Pulsed recovery command, $t_0$ timing does not have any upper limit
- If $t_1$ or $t_2$ exceeds 5us, the recovery command will still be successful, but the transmitter will momentarily turn on.

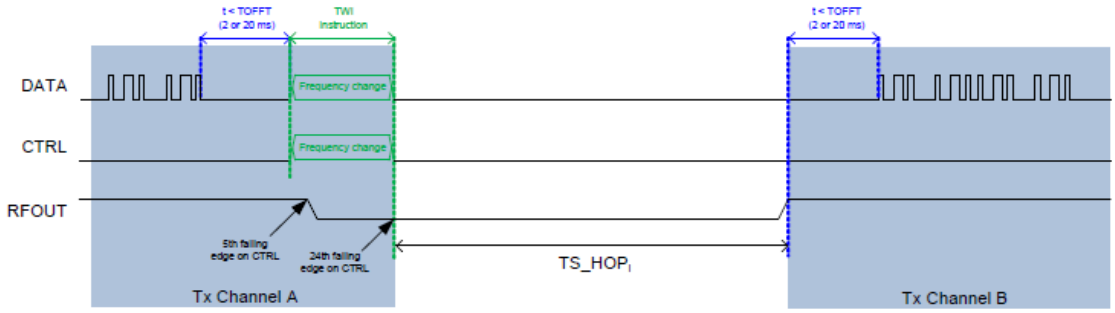
## 1.3. Forced Transmit Mode

In Forced Transmit Mode the circuit can be forced to wake up and go to TX mode by sending an APPLICATION instruction through the 2 wire interface, and setting the Mode bit DA[15] to '1'. Once in Transmit the circuit will transmit over the air the data stream presented on the TX DATA pin. The circuit will stay in transmit mode until a new APPLICATION instruction is sent with DA[15] to '0'. Such behavior is shown in the following timing diagram:




## 1.4. Frequency Hopping Spread Spectrum

Frequency hopping is supported in EXTENDED mode. After sending the data stream in the first channel, the user can send a Frequency change instruction containing the new channel frequency. The circuit will automatically ramp down the PA, lock the PLL to the new frequency, and turn the Power Amplifier back on. The user can then send his packet data on the new channel. Timings are detailed hereafter:




- During any 2 wire interface access, the input of the modulator is inhibited
- The time between two Frequency change instructions shall be greater than $TS\_HOP_i$

## 2. Frequency Band Coverage

The 32001371 TX module offers several combinations or frequency references and frequency outputs, allowing for maximum flexibility and design of multi-band products as shown in the following table:

| Reference Frequency FXOSC | Band Setting DA[13] | Upper/Lower Frequency Bounds | $F_{step}$ | $F_{rf}$ & $F_{dev}$ |
|---|---|---|---|---|
| 26MHz | 0 | 338 to 450MHz | $Fstep = \frac{26x10^6}{2^{14}} = 1.58691kHz$ | $Frf = DF[18:0]xFstep$<br>$Fdev = DA[12:5]xFstep$ |

## 3. Electrical Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FBAND | Accessible Frequency Bands | Band 0 | 338 | - | 450 | MHz |
| FDA | Frequency deviation, FSK | | 10 | - | 200 | kHz |
| BRF | Bit rate, FSK | Permissible Range | 0.5 | - | 100 | kbps |
| BRO | Bit rate, OOK | Permissible range | 0.5 | - | 10 | kbps |
| TS_TR | Time from Sleep to TX mode | | - | 650 | 2000 | us |
| TS_HOP0 | Channel hop time in Band0 | 315 to 390MHz | - | 250 | 500 | us |
| TOFFT | Timer from TX DATA activity to Sleep | Programmable | - | 2<br>20 | -<br>- | ms<br>ms |
| T_START | Time before CTRL pin mode selection | Time from power on to sampling of CTRL | - | 200<br>+TS_OSC | - | ms |

TS_OSC is the oscillator startup time and depends on the electrical characteristics of the crystal.

## 4. Digital Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CTRL}$ | CTRL Clock Frequency | | - | - | 10 | MHz |
| $t_{ch}$ | CTRL Clock High time | | 45 | - | - | ns |
| $t_{cl}$ | CTRL Clock Low time | | 45 | - | - | ns |
| $t_{rise}$ | CTRL Clock Rise time | | - | - | 5 | ns |
| $t_{fall}$ | CTRL Clock Fall time | | - | - | 5 | ns |
| $t_{setup}$ | TX DATA Setup time | From DATA transition to CTRL rising edge | 45 | - | - | ns |
| $t_{hold}$ | TX DATA hold time | From CTRL rising edge to DATA transition | 45 | - | - | ns |
| $t_0$, $t_2$ | Time at logic '1' on DATA during Recovery command | | - | - | 5 | us |
| $t_1$ | Time at logic '0' on DATA during Recovery command | | 5 | - | - | us |